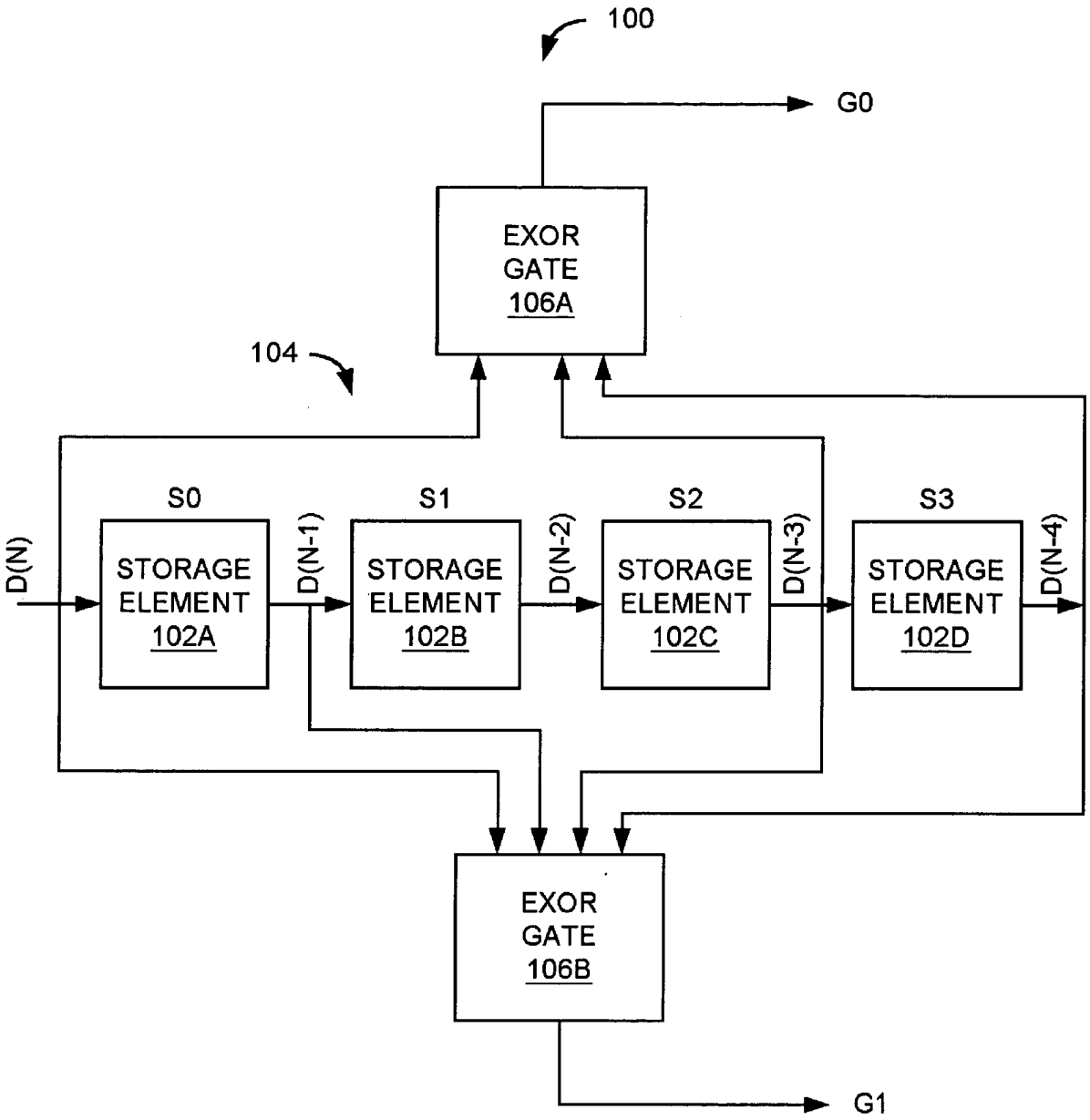

FIG. 1
(PRIOR ART)

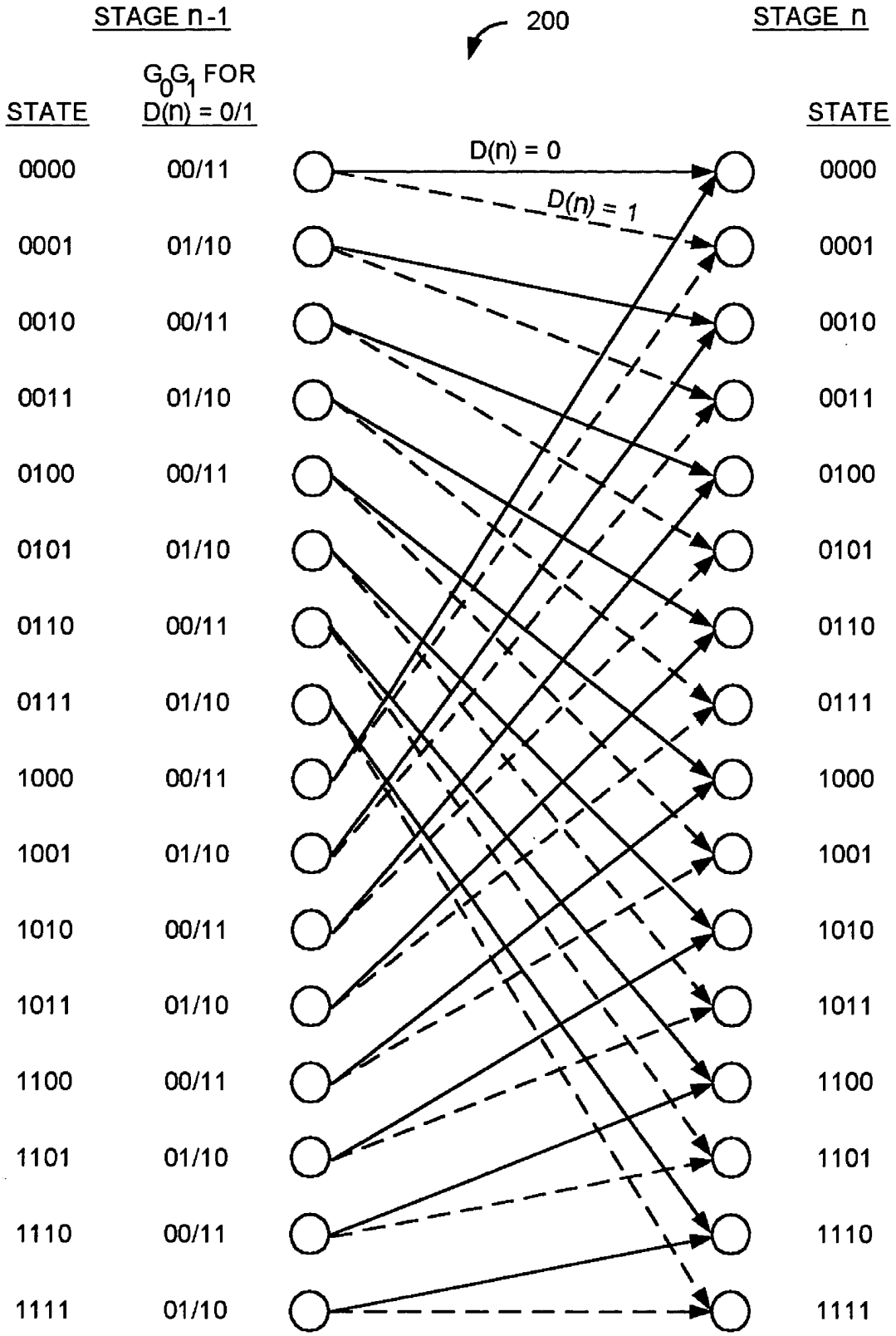

FIG. 2
(PRIOR ART)

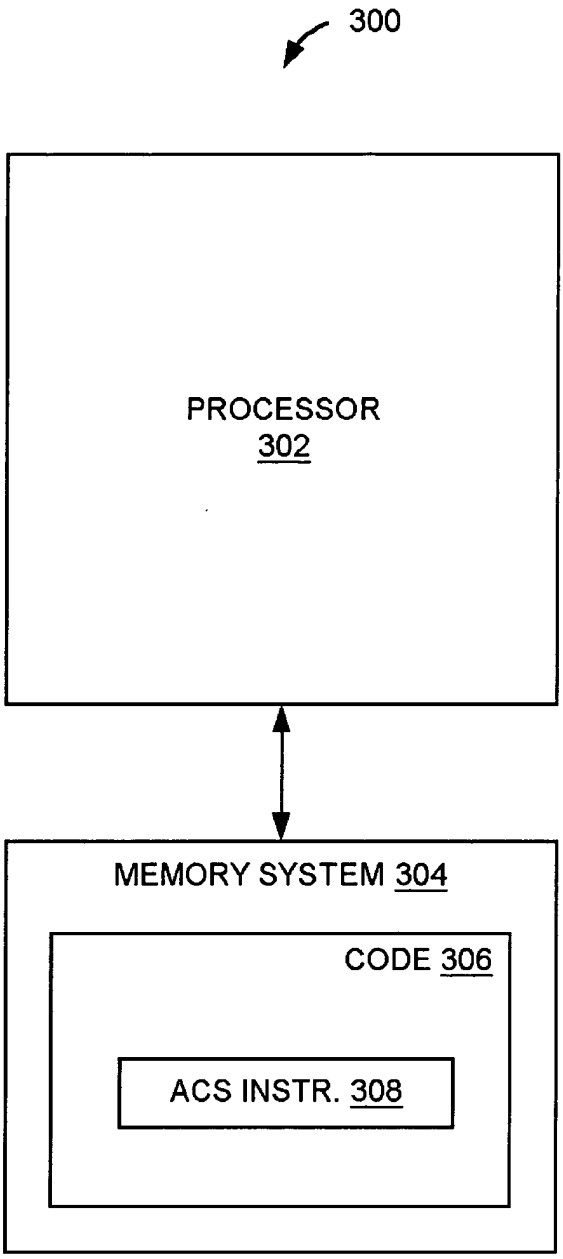

FIG. 3

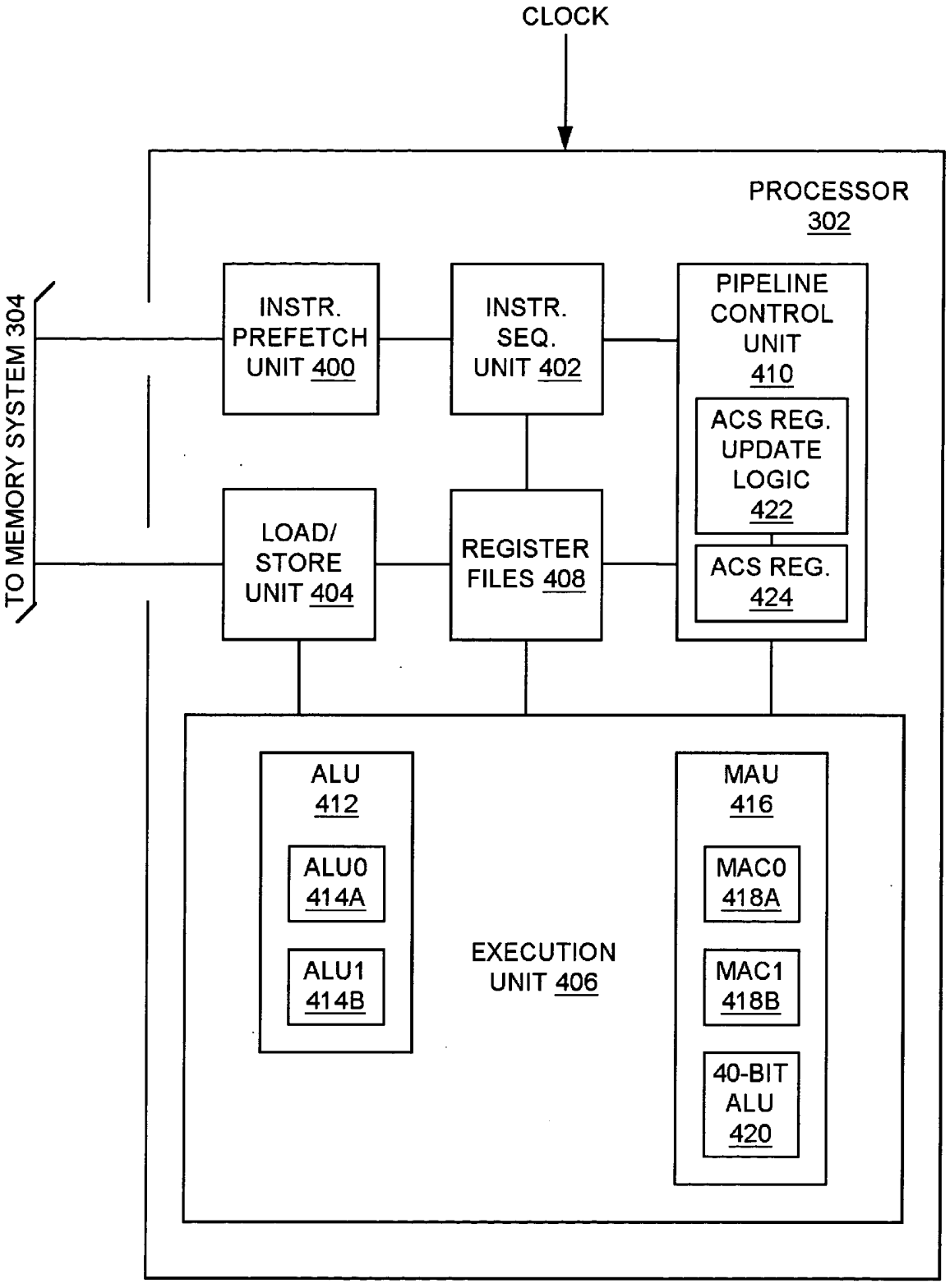
CLOCK
PROCESSOR
302
TO MEMORY SYSTEM 304
INSTR. PREFETCH UNIT 400
INSTR. SEQ. UNIT 402
PIPELINE CONTROL UNIT 410
ACS REG. UPDATE LOGIC 422
ACS REG. 424
LOAD/ STORE UNIT 404
REGISTER FILES 408
ALU 412
ALU0 414A
ALU1 414B
EXECUTION UNIT 406
MAU 416
MAC0 418A
MAC1 418B
40-BIT ALU 420

FIG. 4

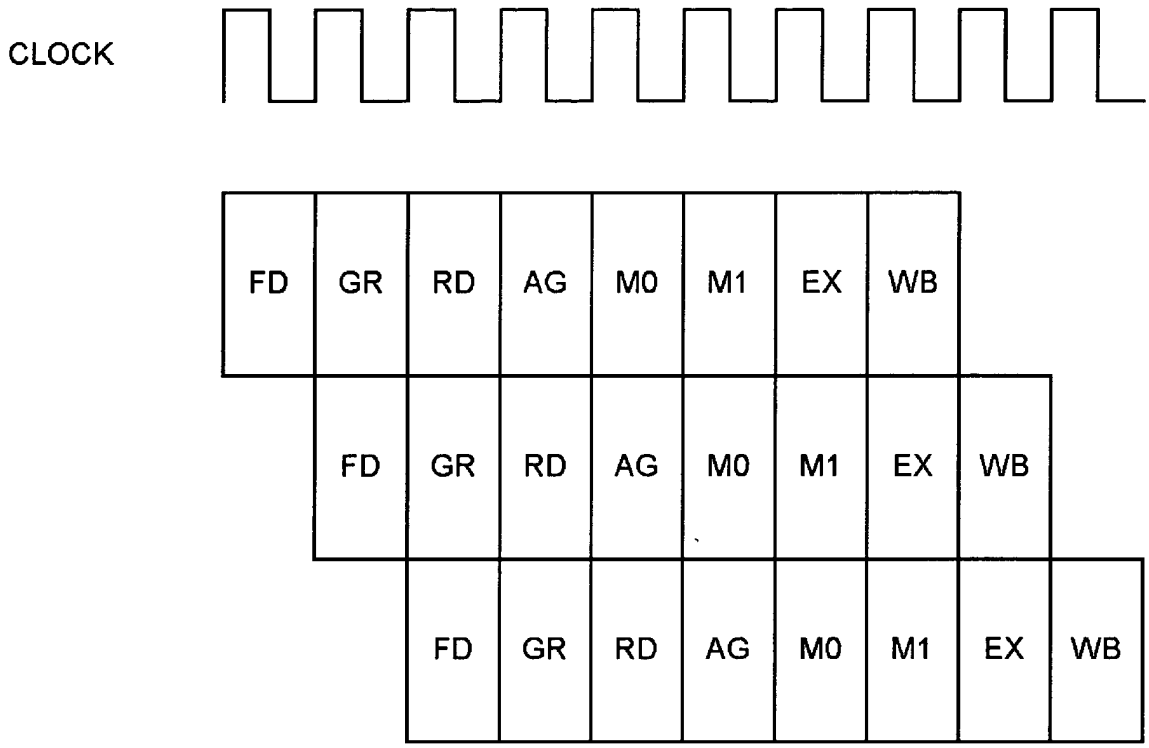

FIG. 5

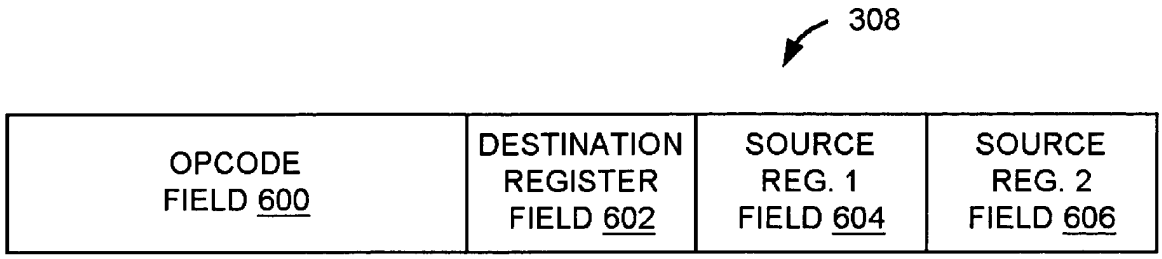

FIG. 6A

REGISTER:

R0	XXXX	
{R5, R4}	0X1123	0X0030
{R7, R6}	0X000A	0X0008
VITR	0X00000000	

FIG. 6B

REGISTER:

R0	0X0038	
{R5, R4}	0X1123	0X0030
{R7, R6}	0X000A	0X0008
VITR	0X00000001	

FIG. 6C

FIG. 7A

REGISTER:

R1	XXXX	
{R5, R4}	0X8000	0XFF30
{R7, R6}	0X000A	0XFF00
VITR	0X00000001	

FIG. 7B

REGISTER:

R1	0X7F00	
{R5, R4}	0X8000	0XFF30
{R7, R6}	0X000A	0XFF00
VITR	0X00000002	

FIG. 7C

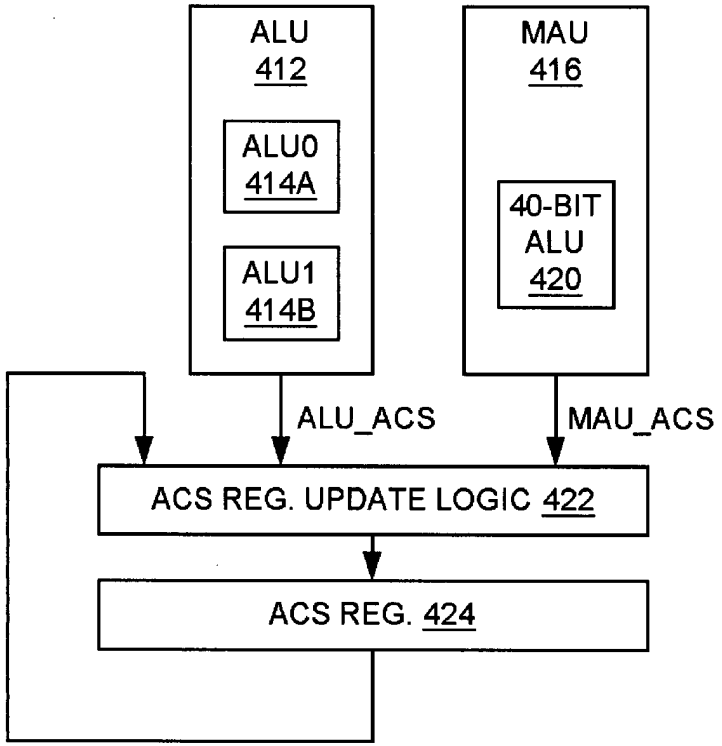
ALU
412
ALU0
414A
ALU1
414B
MAU
416
40-BIT
ALU
420
ALU_ACS
MAU_ACS
ACS REG. UPDATE LOGIC 422
ACS REG. 424

FIG. 8

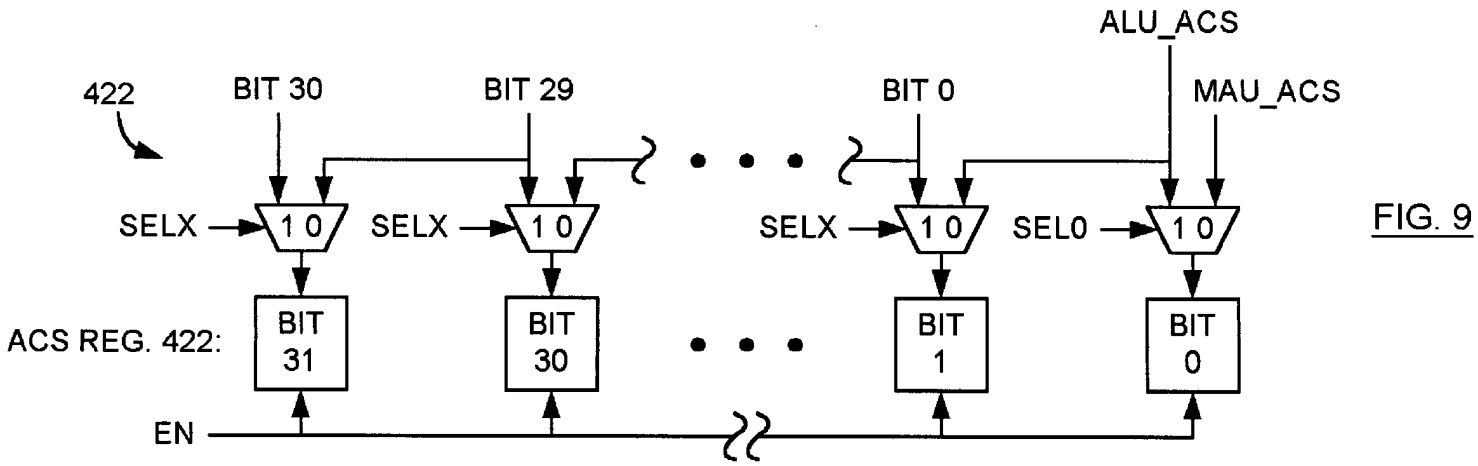
422
BIT 30
BIT 29
BIT 0
ALU_ACS
MAU_ACS
SELX
SELX
SELX
SEL0
1 0
ACS REG. 422:
BIT
31
BIT
30
BIT
1
BIT
0
EN

FIG. 9

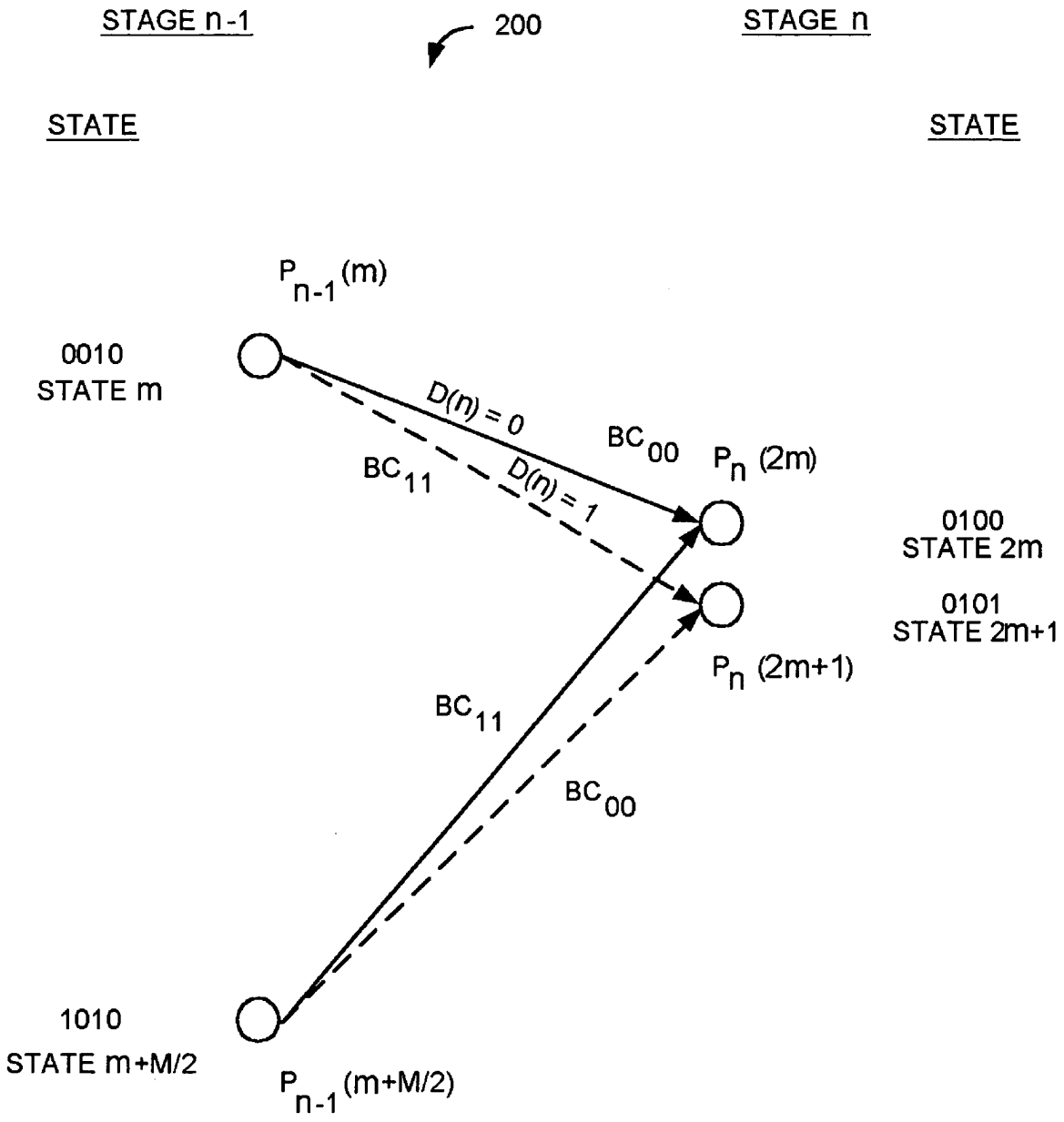
STAGE n-1
200
STAGE n
STATE
STATE
$P_{n-1}(m)$
0010
STATE m
D(n) = 0
BC_{00}
P_n (2m)
BC_{11}
D(n) = 1
0100
STATE 2m
0101
STATE 2m+1
P_n (2m+1)
BC_{11}
BC_{00}
1010
STATE m+M/2
$P_{n-1}(m+M/2)$

FIG. 10

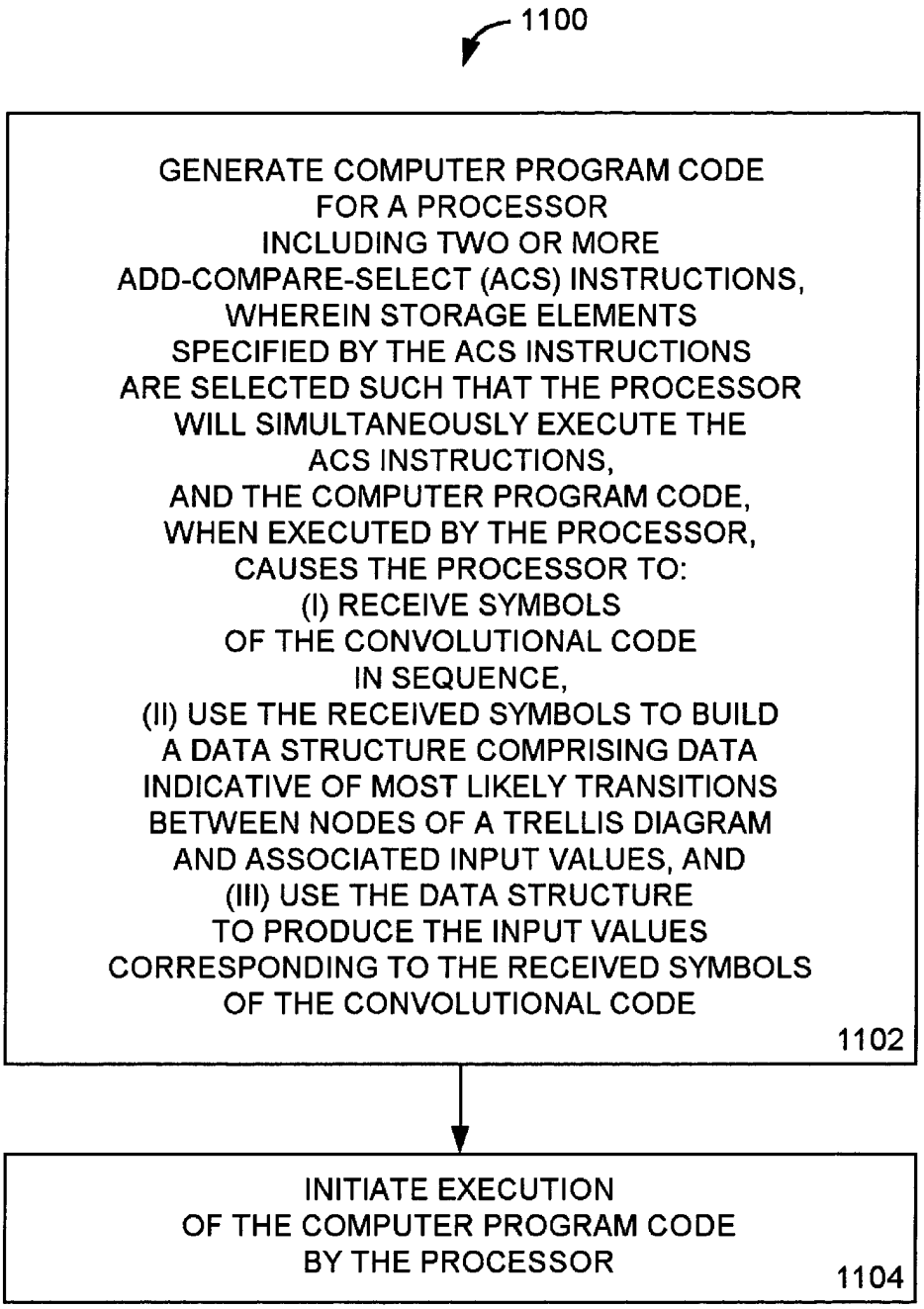
1100
GENERATE COMPUTER PROGRAM CODE FOR A PROCESSOR INCLUDING TWO OR MORE ADD-COMPARE-SELECT (ACS) INSTRUCTIONS, WHEREIN STORAGE ELEMENTS SPECIFIED BY THE ACS INSTRUCTIONS ARE SELECTED SUCH THAT THE PROCESSOR WILL SIMULTANEOUSLY EXECUTE THE ACS INSTRUCTIONS, AND THE COMPUTER PROGRAM CODE, WHEN EXECUTED BY THE PROCESSOR, CAUSES THE PROCESSOR TO: (I) RECEIVE SYMBOLS OF THE CONVOLUTIONAL CODE IN SEQUENCE, (II) USE THE RECEIVED SYMBOLS TO BUILD A DATA STRUCTURE COMPRISING DATA INDICATIVE OF MOST LIKELY TRANSITIONS BETWEEN NODES OF A TRELLIS DIAGRAM AND ASSOCIATED INPUT VALUES, AND (III) USE THE DATA STRUCTURE TO PRODUCE THE INPUT VALUES CORRESPONDING TO THE RECEIVED SYMBOLS OF THE CONVOLUTIONAL CODE
1102
INITIATE EXECUTION OF THE COMPUTER PROGRAM CODE BY THE PROCESSOR
1104

FIG. 11

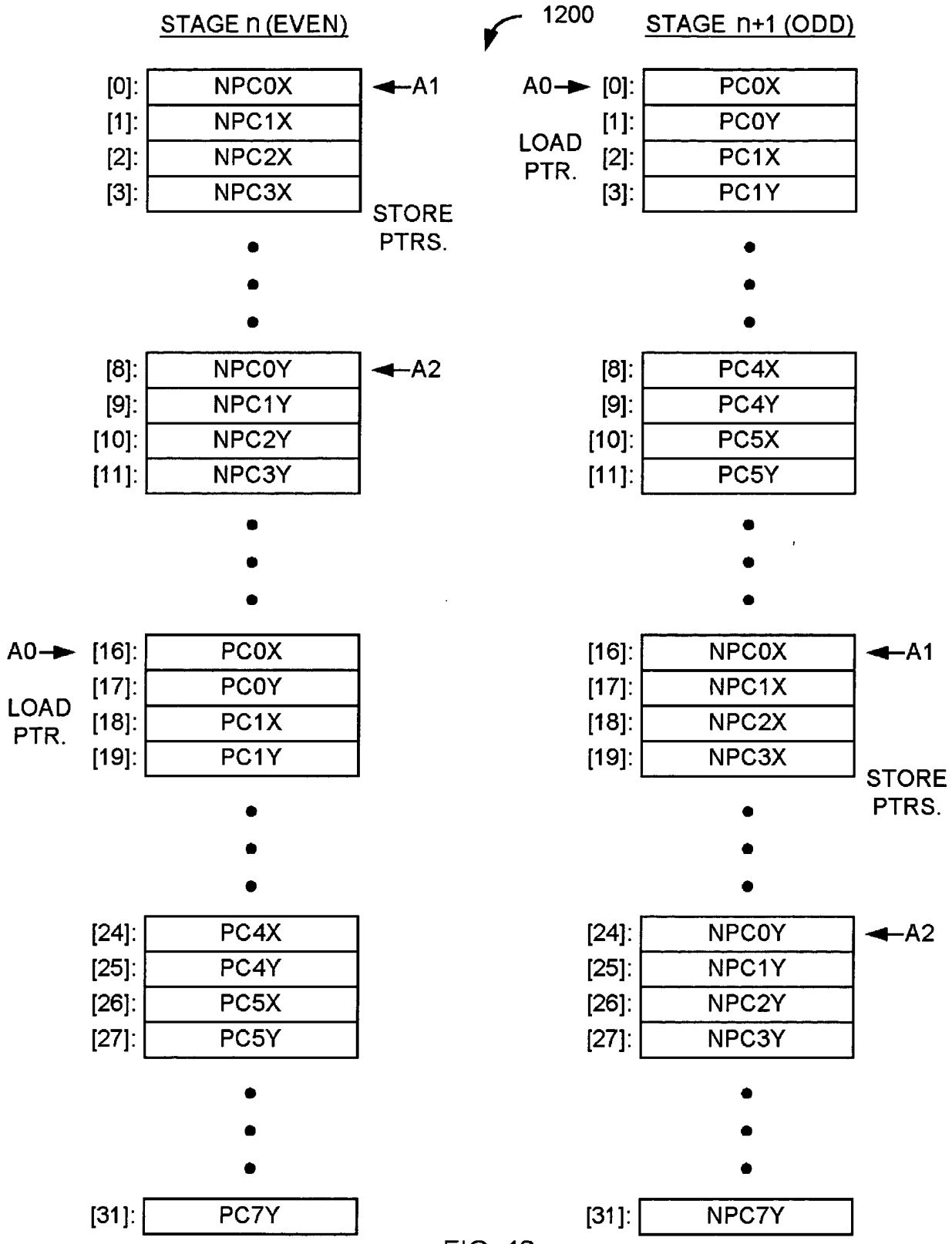
STAGE n (EVEN)
1200
STAGE n+1 (ODD)
[0]: NPC0X
[1]: NPC1X
[2]: NPC2X
[3]: NPC3X
A1
STORE PTRS.
A0
LOAD PTR.
[0]: PC0X
[1]: PC0Y
[2]: PC1X
[3]: PC1Y
[8]: NPC0Y
[9]: NPC1Y
[10]: NPC2Y
[11]: NPC3Y
A2
[8]: PC4X
[9]: PC4Y
[10]: PC5X
[11]: PC5Y
A0
LOAD PTR.
[16]: PC0X
[17]: PC0Y
[18]: PC1X
[19]: PC1Y
[16]: NPC0X
[17]: NPC1X
[18]: NPC2X
[19]: NPC3X
A1
STORE PTRS.
[24]: PC4X
[25]: PC4Y
[26]: PC5X
[27]: PC5Y
[24]: NPC0Y
[25]: NPC1Y
[26]: NPC2Y
[27]: NPC3Y
A2
[31]: PC7Y
[31]: NPC7Y

FIG. 12